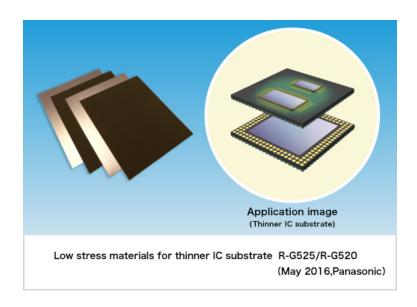


# **Panasonic Corporation**

http://www.panasonic.com/global

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# Panasonic Commercializes a Substrate Material for Semiconductor Packages Featuring Reduced Internal Stress that Leads to Lower Warpage



Panasonic's new substrate material is suited to a wide variety of semiconductor packages, leading to faster material selection and greater design freedom.

Osaka, Japan - Panasonic Corporation announced today that it has developed the MEGTRON GX series (product No. R-G525/R-G520), a substrate material that allows thinner and less expensive semiconductor packages for application to a wide range of semiconductor packages (PoP [1], MCP [2], etc.). Panasonic will start mass-producing the new material in June 2016. This substrate material, the embodiment of a completely new idea, shows reduced internal stress [3] that risks causing warpage, and is applicable to a wide variety of semiconductor packages, allowing faster material selection and improved design freedom. The new product also provides highly reliable connections between IC chips and package substrates.

With mobile equipment becoming ever thinner and more sophisticated, urgent studies are ongoing to develop new types of semiconductor packages. Today, substrate materials with different coefficients of thermal expansion (CTE) [4] are needed for different types of semiconductor packages, making material selection and matching very time-consuming. By utilizing a resin technology designed to minimize internal stress, Panasonic has commercialized a new substrate material that is applicable to a wide range of semiconductor packages.

#### This new product has the following features:

- 1. The substrate material features reduced internal stress, which minimizes warpage, allowing semiconductor packages to be made significantly thinner.
  - •Warpage when heated from 25°C (room temperature) to 260°C: max. 110  $\mu$  m<sup>-1</sup> (Panasonic's conventional product \*2: 235  $\mu$ m)
- 2. The substrate material with reduced internal stress can be used in a wide variety of semiconductor packages.
  - This enables faster selection of semiconductor package substrate materials and gives greater design freedom.
  - •The substrate material can be applied to different types of semiconductor packages (PoP, MCP, SiP [5], etc.), regardless of IC chip size or substrate thickness.
  - (Panasonic's conventional product \*2: In the past, different
  - substrate materials needed to be used in different semiconductor packages
  - that had different specifications.)
- 3. The substrate material eliminates the need for special warp-preventing glass cloth, thus contributing to a cut in the cost of the semiconductor package.
- \*1 This is a measurement for a 160  $\mu$  m-thick substrate and a 100  $\mu$  m-thick chip.
- \*2 R-1515 series (MEGTRON GX series)

### Suitable applications:

The substrate material is for use in thin semiconductor packages incorporated in mobile equipment such as smartphones and tablets.

#### Remarks:

The product will be exhibited at ECTC 2016, held at the Cosmopolitan of Las Vegas in the US from May 31 to June 3, 2016, and at the JPCA Show 2016, held at Tokyo Big Sight, from June 1 to June 3.

#### Detailed description of its features:

1. The substrate material reduces internal stress and minimizes warpage, allowing a reduction in the thickness of semiconductor packages.

The continuing trend of manufacturing thinner semiconductor packages has led to a demand for minimal warpage of package substrate material. Having devised the resin design technology to eliminate internal stress, Panasonic has succeeded in reducing the variation in warpage of the substrate material to 110  $\mu$ m (for a 160  $\mu$ m-thick substrate and a 100  $\mu$ m-thick chip) when the material's temperature is increased from 25°C (room temperature) to 260°C. This substrate material, due to its smaller warpage, assists the manufacture of thinner semiconductor packages.

2. The substrate material that shows reduced internal stress can be used for a wide variety of semiconductor packages. This leads to faster selection of semiconductor package substrate materials and to greater design freedom.

Currently, different types of semiconductor packages (PoP, MCP, etc.) require substrate materials with different CTEs, which take longer to identify and select. The newly developed low-stress substrate material reduces the warpage of IC chips and package substrates, regardless of their thickness or chip sizes, allowing it to be applied to a wide range of semiconductor packages. This speeds up the selection of package substrate material and gives greater design of freedom.

3. The substrate material eliminates the need for special type of stiffening glass cloth, reducing the price of the semiconductor package.

Conventional substrate material includes an insulating layer composed of resin and glass cloth. Low CTE glass cloth, special one is an expensive material that is used to reduce the CTE, but it is the commonest method adopted to suppress warping of the substrate material. The developed substrate material minimizes warpage with the standard glass cloth, not special one due to its newly-adopted resin design technology, thus cutting the cost of the semiconductor package. The new substrate material is applicable to a wide range of semiconductor packages, opening the way to far simpler management of substrate materials inventory with different coefficients of thermal expansion (CTE) for different semiconductor packages.

item 項目		Test method 試験方法	Condition 条件	Unit 単位	MEGTRON (CS) R-G525
Glass transition temp (Tg) ガラス転移温度		DMA*2	A	٣	290
hermal decomposition temp (Td) 熱分解温度		TG/DTA	A	٣	360
CTE x-ax/s 熱影張係数(タテ方向)	σ1	IPC TM-650 2.4.41	A	ppm/°C	4-6
TE y-axis 病數後併數 (日口方向)					4-6
Dielectric constant (Dk) 比誘電率 *1	1642	IPC TM-650 2.5.5.9	C-24/23/50	-	45
Dissipation factor (DF) 誘電正確 *1	1942				0.016
Volume resistivity 体模组抗率		IPC TM-650 2.5.17.1	C-96/35/90	MΩ-cm	1x10°
Surface resistivity 表面组式				МΩ	1x10 <sup>8</sup>
Water absorption 股水率		IPC TM-650 2.6.2.1	D-24/23	%	0.3
Floural modulus 最好弹性率**		JIS C6481	25°C	GPa	1411
			250°C		5
reel strength 開語引き剥がし強さ	1/3oz	IPC TM-650 2.4.8	A	kN/m	0.5

# [Terminology]

#### [1] Package on Package (PoP)

PoP is a structure in which multiple semiconductor packages are stacked on a substrate. It offers the advantages of a smaller packaging area and a shorter wiring length.

[2] Multi-chip Package (MCP)

An MCP is a semiconductor package in which a substrate carries two or more bare chips connected to it. It is also referred to as a multi-chip module.

[3] Stress

Internal stress is defined as the resistance that is created inside an object in response to the application of an external force. A smaller stress results in a lighter load being applied to a connection solder ball when the substrate deforms with heating and cooling.

[4] Coefficient of Thermal Expansion (CTE)

The CTE is a ratio that describes the increase in length, at constant pressure, of a material per unit temperature during a temperature change.

[5] System in Package (SiP)

SiP is a semiconductor package constructed by mounting a CPU, memories, and other chips on a substrate and interconnecting them through wires to allow the package to function as an integrated system.

## **About Panasonic**

Panasonic Corporation is a worldwide leader in the development of diverse electronics technologies and solutions for customers in the consumer electronics, housing, automotive, enterprise solutions and device industries. Since its founding in 1918, the company has expanded globally and now operates 474 subsidiaries and 94 associated companies worldwide, recording consolidated net sales of 7.553 trillion yen for the year ended March 31, 2016. Committed to pursuing new value through innovation across divisional lines, the company uses its technologies to create a better life and a better world for its customers. To learn more about Panasonic: http://www.panasonic.com/global.

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