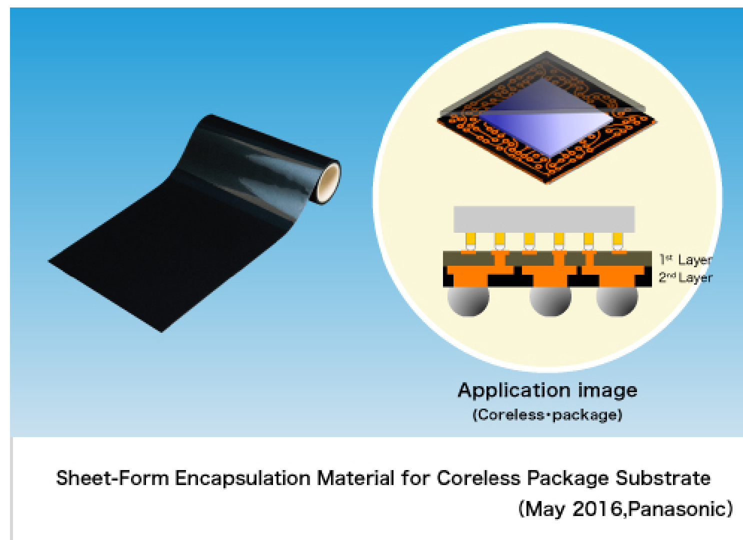
May 26, 2016

Panasonic Commercializes "Sheet-Form Encapsulation Material for Coreless Package Substrates"



Sheet-Form Encapsulation Material for Coreless Package Substrate
(May 2016,Panasonic)

Panasonic's new material for coreless package substrates is suited for the insulation layer of semiconductor package substrates.

Osaka, Japan - Panasonic Corporation announced today that it has developed a sheet-form encapsulation material (CV2008 series) for coreless package substrates [1] that enables thinner-profile and lower-cost semiconductor packages. The sheet-form encapsulation material, scheduled for mass production from June 2016, is optimized for the insulation layers of coreless package substrates. Its suitability for large-area encapsulation allows thinner packages to be manufactured at lower cost.

With the increasing compact-sizing and ever-higher functionality of mobile terminals such as smartphones, the packages used in these products need to have thinner profiles and lower cost. One noticeable response to this demand has been to develop a new coreless process that differs from the current mainstream buildup process using thin core materials[2]. The market requires an insulation material for coreless processes that shows good productivity and eliminates the need for thin core materials as well as laser drilling processing. Panasonic has responded by using its resin design technology to develop a sheet-form encapsulation material for coreless package substrates.

This new product has the following features:

1. A sheet-form encapsulation material with a uniformly produced insulation layer thickness is ideal for the new coreless process*1, as it eliminates the need for laser drilling processing. The insulation layer for a package substrate can be produced using a large-area press process, enabling the mass production of packages at lower cost.
   - Sheet thickness is available in the range of 20 - 200 µm.
2. The high rigidity of the thin sheet encapsulation material minimizes any warpage of packages and contributes to a thinner profile. Modulus of elasticity: 17000 MPa at 25˚C.
3. A low shrinkage rate of material ensures connection reliability to be maintained during high-temperature reflow processes, increasing the production yield of the package assembly process.
   - Shrinkage rate: 0.003%*2

*1: Copper pillar resin encapsulation process

*2: Shrinkage rate before and after IR reflow at up to 250˚C, 4 passes (JIS-K6911)

Suitable applications:

Copper pillar resin encapsulation type coreless package substrates, etc.

Remarks:

This product will be exhibited at ECTC 2016, to be held at The Cosmopolitan of Las Vegas, Nevada, USA, from May 31 to June 3, 2016.

Detailed description of its features:

1. A sheet-form encapsulation material with a uniformly produced insulation layer thickness is ideal for the new coreless process, as it eliminates the need for laser drilling processing. The insulation layer for a package substrate can be produced using a large-area press process, enabling the mass production of packages at lower cost.

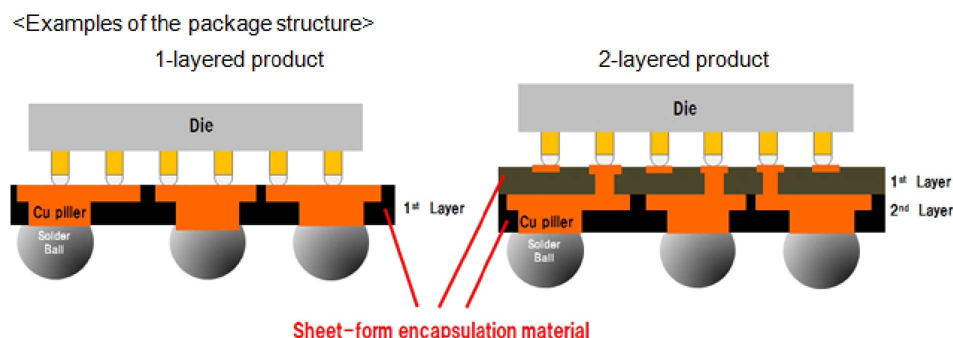
Conventional package substrates are produced from thin core material including glass cloth, and via [3] forming requires laser drilling processing and through-hole copper plating for connection between both surfaces, resulting in a high-cost process. In contrast, a coreless package substrate using the new copper pillar resin encapsulation process [4] can produce copper pillars by copper plating employing an additive process that eliminates the need for laser drilling processing, leading to a thinner package profile and lower cost. To enable the mass production of package substrates, an easily-managed material is needed that allows the press-forming of a uniform insulation layer over a large area. Panasonic has commercialized a product featuring sheet-formed encapsulation material of uniform thickness that is optimized for coreless processes by applying a unique filler design and proprietary resin design technology. Adoption of this material for the insulation layer enables press forming over a large area, contributing to the mass production of packages at lower cost. Sheet thicknesses from 20 µm to 200 µm can be produced for the wide variety of package types required by customers.

2. The high rigidity of the thin sheet encapsulation material minimizes any warpage of packages and contributes to a thinner profile.

A coreless package substrate carries the risk of increased warpage if its insulation layer is very thin, risking handling problems during the assembly process. To secure reliability in the assembly process, minimal warpage is required, especially for a thin material. The company's unique filler design and resin design technology have achieved high rigidity and strength even with extremely thin sheets, reducing package warpage while maintaining a thin profile.

3. A low shrinkage rate of material ensures connection reliability to be maintained during high-temperature reflow processes, increasing the production yield of the package assembly process.

Since the package assembly process may undergo multiple high temperature reflow processes, a smaller thermal shrinkage rate is required for package substrate materials to prevent bonding defects between the conductor on the substrate and the IC chip. This material has achieved a low shrinkage rate by developing a unique filler design technology that will achieve improved production yield in the assembly process.



Notes:

[1] Coreless package substrate
A type of semiconductor package substrate that does not use a thin core material (copper-clad laminated board). Coreless package substrates are attracting increasing attention as a replacement for the conventional buildup substrate used for semiconductor packages. A buildup substrate consists of a buildup layer on both sides of a thin core material to support the semiconductor elements, but a coreless package eliminates the thin core material.
[2] Thin core material (copper-clad laminated board)
Produced from glass-fiber cloth, impregnated with epoxy resin, and laminated with copper foil on both sides by thermocompression bonding. A conventional package substrate contains a thin core material.
[3] Via
An electrical connection made between top-layer and bottom-layer wiring in a multi-layer wiring board
[4] Copper pillar resin encapsulation process
A type of coreless package substrate in which copper pillars are initially formed in a additive process, after which an insulation layer is formed.

About Panasonic

Panasonic Corporation is a worldwide leader in the development of diverse electronics technologies and solutions for customers in the consumer electronics, housing, automotive, enterprise solutions and device industries. Since its founding in 1918, the company has expanded globally and now operates 474 subsidiaries and 94 associated companies worldwide, recording consolidated net sales of 7.553 trillion yen for the year ended March 31, 2016. Committed to pursuing new value through innovation across divisional lines, the company uses its technologies to create a better life and a better world for its customers. To learn more about Panasonic: http://www.panasonic.com/global.

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